REMARKS/ARGUMENTS

Claims 11-20 and 22-37 are pending in this application. By this Amendment, Applicants amend claims 14, 15 and 23 and add new claims 35-37.

Claims 11-17, 22, 23, 26-31 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over A.G.P. Interface Specification Revision 1.0 by Intel in view of Dye (U.S. 6,370,631). Claims 11-17, 22, 23, 26-31 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Intel in view of Dye, and further in view of Lentz (U.S. 5,649,173).

Applicants note that although the Examiner listed claims 11-17, 22, 23, 26-31 and 34 in the rejection over Intel in view of Dye, it appears that the Examiner intended to reject claims 11-17, **20**, 22 ,23, 26-31 and 34 over Intel in view of Dye, since each of claims 11-17, 20, 22, 23, 26-31 and 34 are specifically discussed in this rejection.

In addition, although the Examiner listed claims 11-17, 22, 23, 26-31 and 34 in the rejection over Intel in view of Dye, and further in view of Lentz, it appears that the Examiner intended to reject claims 18, 19, 24, 25, 32 and 33 over Intel in view of Dye, and further in view of Lentz, since each of claims 18, 19, 24, 25, 32 and 33 were specifically discussed in this rejection.

Applicants respectfully traverse these rejections.

Claim 14 has been amended to recite:

> "An apparatus for image processing, comprising:
> a processor including a data decompression circuit;
> a first storage device having texture data and electronically coupled to said processor; and
> **a texture buffer having decompressed texture data and being directly connected to said processor**; wherein
> transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor; and
> said first storage device is defined by a CPU work memory or an external memory device." (emphasis added)

Claims 15 and 23 recite features that are similar to the features recited in claim

14, including the above-emphasized features.

The Examiner alleged that Intel teaches all of the features recited in claims 14, 15 and 23, except for a processor including a data decompression circuit. The Examiner further alleged that Dye teaches a memory controller IMC and the IMC Block Diagram discloses FIFO means, codec engine, and texture mapping logic, respectively. Thus, the Examiner concluded that it would have been obvious "to utilize the memory controller (IMC) for specialized codec engine means of DYE to modify the AGP Interface teaching as disclosed above in INTEL because use of the codec engine of DYE provides (1) improved performance (see col. 2, lines 40-44); (2) the IMC also improves overall system performance and response using main system memory for graphical information and storage and also reduces bandwidth requirements for graphical displays (see col. 2, lines 52-67)." Applicants respectfully disagree.

Claim 14 has been amended to recite the feature of "a texture buffer having decompressed texture data and **being directly connected to said processor**" (emphasis added). Claims 15 and 23 have been similarly amended. Support for these claim amendments can be found in Fig. 6 of the originally filed application and its corresponding description, which discloses a texture buffer 104 which is directly connected to the image processing unit 101.

First, in contrast to the Examiner's allegations, Intel fails to teach or suggest any texture buffer. The Examiner alleged that LFB of Intel corresponds to a texture buffer. However, this is clearly incorrect. The LFB of Intel is clearly a **frame buffer**, **NOT** a **texture buffer**. In fact, Intel fails to teach or suggest any texture buffer whatsoever. Thus, Intel certainly fails to teach or suggest the feature of "a texture buffer having decompressed texture data and being directly connected to said processor" as recited in Applicants' claim 14, and similarly in Applicants' claims 15 and 23.

Second, even assuming *arguendo* that the LFB of Intel could be fairly construed as a texture buffer as recited in Applicants' claims 14, 15 and 23, Intel still fails to teach or suggest the feature of "a texture buffer having decompressed texture data and being directly connected to said processor" as recited in Applicants' claim 14, and similarly in

Applicants' claims 15 and 23. Particularly, as seen in Fig. 2-3 of Intel, the LFB of Intel is connected to a Graphics Accelerator (Gfx Accel) which is connected via the AGP to the Processors (Proc.), and is clearly **NOT directly connected** to any processor. Thus, Intel certainly fails to teach or suggest the feature of "a texture buffer having decompressed texture data and being directly connected to said processor" as recited in Applicants' claim 14, and similarly in Applicants' claims 15 and 23.

Third, contrary to the Examiner's allegations, Applicants respectfully submit that Dye **cannot** be combined with Intel. Dye teaches an IMC (Integrated Memory Controller) which is a PCI bus. The IMC integrates the functions of a graphics adapter and a memory controller to improve performance by transferring data between a CPU and the System Memory in compressed or decompressed format. In contrast, the AGP of Intel is "physically, logically, and electrically independent of the PCI bus.... The add-in slot defined for A.G.P. uses a new connector body (for electrical signaling reasons) which **is not compatible with the PCI connector; PCI and A.G.P boards are not mechanically interchangeable**" (emphasis added).

Thus, contrary to the Examiner's allegations, the image processing device of Intel including the physically, logically, and electrically independent A.G.P. clearly could not have been modified so as to include the IMC of Dye, because (1) the A.G.P of Intel is specifically used only for image display devices, whereas the IMC of integrates the functions of a graphics adapter and a memory controller; and (2) the IMC of Dye is a PCI bus which **in not interchangeable with the A.G.P.** of Intel.

Therefore, Applicants respectfully submit that it would not have been obvious to modify the device of Intel to include the IMC of Dye, as alleged by the Examiner.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 11-17, 20, 22, 23, 26-31 and 34 under 35 U.S.C. § 103(a) as being unpatentable over Intel in view of Dye.

The Examiner relied upon Lentz to allegedly cure various deficiencies of Intel and Dye. However, Lentz clearly fails to teach or suggest the feature of "a texture buffer having decompressed texture data and being directly connected to said processor" as

recited in Applicants' claim 14, and similarly in Applicants' claims 15 and 23.

Accordingly, Applicants respectfully submit that Intel, Dye and Lentz, applied alone or in combination, fail to teach or suggest the unique combination and arrangement of features recited in Applicants' claims 14, 15 and 23.

In view of the foregoing amendments and remarks, Applicants respectfully submit that Claims 14, 15 and 23 are allowable. Claims 16-20, 22 and 24-37 depend upon claims 14, 15 and 23, and are therefore allowable for at least the reasons that claims 14, 15 and 23 are allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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Attorneys for Applicant

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

KEATING & BENNETT LLP
8180 Greensboro Drive, Suite 850
Tyson's Corner, VA 22102
Telephone: (703) 637-1480
Facsimile: (703) 637-1499